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Docket: AM-6569.P1

Amendments to the Specification

Paragraph at page 1, lines 5-8:

This application is a continuation in part of International Application PCT/US02/36940, filed November 14, 2002, which is a continuation in part of Serial No. 09/993,543, filed November 14, 2001, now issued ~~fee paid~~ as U.S. Patent 6,610,184, both of which are incorporated by reference herein in their entireties.

Paragraph at page 2, lines 5-31:

Prior to via metallization, a liner layer 20 is deposited over the top surface of the dielectric layer 14 and on the bottom wall and side walls of the via hole. The liner layer 20 [[14]] performs several functions including a barrier to diffusion between the via metal and the oxide dielectric, an adhesion layer between the oxide and metal, and a seed or nucleation layer for after deposited metal. Although aluminum was the dominant metallization in the past, copper in a dual-damascene structure is beginning to dominate advanced integrated circuits because of its lower electrical resistivity and electromigration and the ability to fill the via hole 16 with copper using of electro-chemical plating (ECP). In the case of copper, the conductive feature 10 is typically the trench portion of a dual-damascene metallization. The liner layer 20 for copper typically includes a barrier layer of tantalum nitride (TaN), an adhesion layer of Ta. A thin copper seed layer both nucleates the ECP copper and serves as an electrode for the electro-chemical process. Chemical vapor deposition (CVD) or its improvement of atomic layer deposition (ALD) may be used for some of the layers. Both techniques tend to coat conformal layers in high aspect-ratio holes, and ALD can coat very thin layers of compounds. However, sputtering is typically preferred because of its economy and good film quality if several inherent problems can be overcome. Sidewall coverage is generally poor and produces thin sidewall portions 22 deep inside the hole 16. Sputtering tends to form overhangs 24 at the top of the hole 16, which at a minimum increase the effective aspect ratio for thereafter coating into the hole 16

and at worst bridge over the top of the hole 16, preventing any further deposition into the hole 16. Various techniques incorporating electrically biasing the wafer can be used to reduce the overhangs 24 and to increase the sidewall coverage. These techniques tend to enhance the bottom coverage, as represented by a thicker bottom portion 26. However, the bottom portion 26 stands in the conductive path to the lower conductive feature. Tantalum, although a metal, has a somewhat high electrical resistivity. Tantalum nitride is significantly resistive. As a result, it is desired to etch away the bottom portion 26. On the other hand, etching of the overhangs 24 should not remove underlying barrier layers.

Paragraph at page 4, line 25 to page 5, line 4:

When the coil 70 is negatively biased, it attracts the argon ions to sputter tantalum from the coil 70. When the coil 70 is driven by RF power it generates an axial RF magnetic field which induces an azimuthal electric field to induce a plasma region in the lower portion of the chamber 30. That is, the secondary plasma source creates a disk-shaped region of argon ions close to the wafer. Another RF power supply 78 is coupled through a capacitive coupling circuit 80 to the pedestal electrode 38, which induces a negative DC self-bias at the edge of the adjacent plasma. As a result, the argon ions in the secondary plasma source, as well as any from the top magnetron/target source, are accelerated to the wafer 40 and sputter etch it. Because of the anisotropy produced by the acceleration, the energetic ions reach to the bottom of the via holes and are effective at selectively etching the bottom portion 26 relative to the sidewall portion 22.

Paragraph at page 5, lines 23-29:

The coil 70 needs to be supported inside not only the electrically grounded chamber walls 30 but also inside the grounded sputtering shields used not only to protect the walls from deposition but also to act as an anode in opposition to the cathode target 34. A simple, easily serviceable mechanical system is needed ~~need~~ to support the coil and provide electrical connections to it. A further problem, particularly with the recently developed 300mm chambers, is that the size of the chamber needs to be minimized to reduce the foot print of the reactor in

valuable clean room space.

Paragraph at page 7, line 24 to page 8, line 10:

A mechanism believed to be responsible for the non-uniform rate will be explained with reference to the schematic illustration of FIG. 4. The RF inductive coil 70 creates an initial plasma distribution 80 that is largely concentrated near the coil 70. The edge localization is explainable in terms of the skin depth of the plasma being created. The RF coil 70 produces an RF magnetic field generally along the central axis 32. The RF magnetic field in turn generates an azimuthal electric field which excites an azimuthal current which in turn supports the plasma and increases its density. However, the electric field in turn is electrically shorted by the highly conductive plasma. That is, the RF field reaches into the plasma only to the skin depth of the plasma. However, the plasma diffuses, as shown by distribution 82, in the axial direction towards the wafer 40 and also radially. The radial diffusion includes inward components towards the central axis 32 and outward components towards the coil 70, which sinks any electrons striking the electrically driven coil 70. In a neutral plasma, the ion density follows that of the electrons. The edge loss effectively ~~effective~~ sharpens into a subsequent distribution 84, in which the edge drains electrons previously diffused to the center 32. As a result, when the plasma strikes the wafer 40, the distribution of the plasma density decreases from a maximum at the center 32 towards the edge of the wafer 40. This plasma density distribution is directly reflected in the sputter etching rate.